WHAT IS CLAIMED IS:

1. A RAM memory with a shared SA structure, comprising:

a plurality of sense amplifiers configured as differential amplifiers and arranged in SA strips, each between adjacent memory cell blocks; and

isolation transistor pairs for connecting sense amplifiers and at least one of a plurality of bit line pairs of respective adjacent memory cell blocks in response to a connection control signal;

wherein the sense amplifiers are arranged in each case jointly for at least four bit line pairs of the adjacent memory cell blocks, such that each of the bit line pairs is assignable to a respective sense amplifier to be connected to a different memory cell in the respective cell block by means of word line signals fed via a common word line.

2. The RAM memory as in claim 1, wherein a first and a second memory cell sharing a common word line, and connected to a first and second bit line pair, respectively, each assigned to the same sense amplifier of the same cell block, in each case have a first and second selection transistor, are provided such that a word line signal of a first level on the common word line selects a first of the two memory cells and connects it to the bit line pair associated with it, and isolates the second memory cell from the bit line pair associated with it and a word line signal of a second, different level on the same word line isolates the first memory cell from the bit line pair associated with it and connects the other memory cell to the bit line pair associated with it.

3. The RAM memory in claim 2, wherein the first selection transistor is a PMOS transistor and the second selection transistor is an NMOS transistor and the first level of the word line signal is a low level and the second level of the word line signal is a high level.

4. The RAM memory as claimed in claim 1, wherein a first and second isolation transistor pair of the same cell block are in each case set up for a first and second bit line pair assigned to the same sense amplifier, wherein a connection control signal set at a first level fed to them via a common connection control signal line, connects the first of the two bit line pairs to the same sense amplifier and isolates the second bit line pair from said sense amplifier, and a connection control signal set at a second level on the same connection control signal line isolates the first bit line pair from the same sense amplifier and connects the second bit line pair to the common sense amplifier.

5. The RAM memory in claim 1, wherein the first isolation transistor pair comprises PMOS transistors and the second isolation transistor pair comprises NMOS transistors and the first level of the connection control signal is a low level and the second level of the connection control signal is a high level.

6. The RAM memory as claimed in claim 2, further comprising a control device for connecting a bit line pair selected from the first and second bit line pair of the same cell block to the common sense amplifier in a connection interval, wherein the control device generates the word line signal on the associated word line and the connection control signal for said bit line pair on the associated connection control signal line, wherein the connection control signal lies

within the time interval of the word line signal and, during the same time interval, applies a center level to the connection control signal line leading to the isolation transistor pairs of the bit line pairs of the adjacent cell block that are assigned to the same sense amplifier–, which center level deactivates said line.

7. A RAM memory with a shared sense amplifier structure comprising:

a sense amplifier strip containing a plurality of sense amplifiers, wherein the sense amplifier strip is deposed between, and in communication with, a first and a second cell block;

a first connection control signal line residing in the first cell block;

a second connection control line residing in the second cell block;

a first word line, residing in the first cell block and coupled to a first and a second memory cell;

a second word line, residing in the second cell block, and coupled to a third and a fourth memory cell;

a first bit line pair residing in the first cell block and coupled to the first connection control signal line;

a second bit line pair residing in the first cell block and coupled to the first connection control signal line;

a third bit line pair residing in the second cell block and coupled to the second connection control signal line; and

a fourth bit line pair residing in the second block and coupled to the second connection control signal line,

wherein, at any one instant, a single pair of the first, second, third or fourth bit line pairs can be connected to a common sense amplifier residing in the sense amplifier strip.

8. The memory of claim 7, wherein the sense amplifiers residing in the sense amplifier strip are configured as differential amplifiers.

9. The RAM memory of claim 8, further comprising:

a first selection transistor coupled to the first word line and the first memory cell; and

a second selection transistor coupled to the first word line and the second memory cell,

wherein a signal on the first word line set at a first level connects the first cell to the first bit line pair, and wherein the signal on the first word line set at a first level isolates the second memory cell from the second bit line pair.

10. The RAM memory of claim 9, wherein a signal on the first word line set at a second level isolates the first cell from the first bit line pair, and wherein a signal on the first word line set at a second level connects the second memory cell to the second bit line pair.

11. The RAM memory of claim 9, further comprising:

a third selection transistor coupled to the second word line and the third memory cell; and

a fourth selection transistor coupled to the second word line and the fourth memory cell,

wherein a signal on the second word line set at a first level connects the third cell to the third bit line pair, and wherein a signal on the second word line set at a first level isolates the fourth memory cell from the fourth bit line pair.

12. The RAM memory of claim 11, wherein a signal on the second word line set at a second level isolates the third cell from the third bit line pair, and wherein a signal on the second word line set at a second level connects the fourth memory cell to the fourth bit line pair.

13. The RAM memory as claimed in claim 12, wherein

the first and third selection transistors are PMOS transistors and the second and fourth selection transistors are NMOS transistors, and wherein the first level is a low level and the second level is a high level.

14. The RAM memory of claim 8, further comprising:

a first pair of isolation transistors coupled to the first connection control signal line; and

a second pair of isolation transistors coupled to the first connection control signal line, wherein a signal on the connection control signal line set at a first level connects the first bit line pair to the common sense amplifier, and wherein a signal on the first connection control signal line set at a first level isolates the second bit line pair from the common sense amplifier.

15. The RAM memory of claim 14, wherein a signal on the first connection control signal line set at a second level isolates the first bit line pair from the common sense amplifier, and wherein a signal on the first connection control signal line set at second level connects the second bit line pair to the common sense amplifier.

16. The RAM memory of claim 14, further comprising:

a third pair of isolation transistors coupled to the second connection control signal line; and

a fourth pair of isolation transistors coupled to the second connection control signal line, wherein a signal on the second connection control signal line set at a first level connects the third bit line pair to the common sense amplifier, and wherein a signal on the second connection control signal line set at a first level isolates the fourth bit line pair from the common sense amplifier.

17. The RAM memory of claim 16, wherein a signal on the second connection control signal line set at a second level isolates the third bit line pair from the common sense amplifier, and wherein a signal on the second connection control signal line set at a second level connects the fourth bit line pair to the common sense amplifier.

18. The RAM memory of claim 17, wherein the first and third isolation transistor pairs are PMOS transistors and the second and fourth isolation transistor pairs are NMOS transistors, and wherein the first level of the connection control signal is a low level and the second level of the connection control signal is a high level.

19. The RAM memory of claim 8, further comprising a control device, wherein the control device is coupled to the first word line, the second word line, the first connection control signal line, and the second connection control signal line.

20. The RAM memory of claim 19, wherein the control device generates a word line signal on the first word line and a connection control signal on the first connection control signal line, and

wherein the connection control signal lies within the time interval of the word line signal, and wherein, during the same time interval, the control device applies a center level to the second connection control signal line, wherein the center level deactivates the second connection control signal line, whereby a bit line pair chosen from the first and second bit line pair is connected to the common sense amplifier during a connection interval.